

Examiner – Joseph Nguyen

Applicant – Edlin Solomon
Application 09/871,383(20020089000-A1).
Mailing date 9.27.2002.
Reply mailed 12.05.2004.

Reply No.12 to Notice received on 10.18.2002.

RECEIVED
DEC 13 REC'D

H01L 29/06 TC 2800
H01L 29/70

BIDIRECTIONAL BIPOLAR STATIC INDUCTION TRANSISTOR

The invention relates to microelectronics and more particularly to bidirectional bipolar static induction devices: transistor and transistor-triac (transistor, which can be latched) with elements of a control circuit. Any device, according to the present invention can be latched. However, if the latch current of the device exceeds the maximum permissible constant current, such device can be considered as the device without latching, i.e. the transistor.

background of the invention

There exists a method for fabricating a semiconductor device including the steps of: forming a gate insulation film on the upper surface of a semiconductor substrate; forming a polysilicon layer; forming a dummy layer pattern on the upper surface of the polysilicon layer; forming a polysilicon layer pattern; forming an insulating side wall spacer on both side walls of the dummy layer pattern; injecting an impurity ion into the semiconductor substrate of the both sides of the side wall spacer, to form a source and a drain; forming an insulation layer in a manner that the entire upper surface of the semiconductor substrate becomes higher than the dummy layer pattern; performing a chemical-mechanical polishing step, to expose the upper surface of the dummy layer pattern; etching the dummy layer pattern and forming a trench on the gate insulation film; forming a barrier film on the inner wall of the trench and on the upper surface of the insulation layer; and filling the trench with copper layer[1].

There exists a vertical JFET, in which a gate and a channel are formed by the implantation of an impurity in a doped epitaxial layer through mask – a doped polysilicon source electrode[2]. The method provides forming of the transistor with channel thickness equals about 10.^{sup.}-5 cm.

There exists a bipolar static induction transistor comprising elements of a bipolar static induction transistor: a gate, a source and a channel – on one of the sides of the substrate, and elements of a onejunction transistor: an emitter and a base (drain) – on the other [3]. This transistor has high current density and can switch relatively high power.

There exists a static induction type semiconductor device comprising a semiconductor region having one conductivity type and a low impurity concentration and gate regions having an opposite conductivity type and a high impurity concentration formed in the semiconductor region to thereby define a channel region between these gate regions, there is provided a subsidiary semiconductor region having the one conductivity type and a relatively high impurity concentration either around each gate region to leave an effective channel region in the semiconductor region, or adjacent to the effective channel region in the entire channel region on the drain side. By so constructing the device, this effective channel region has a relatively low potential difference even when the channel region is completely depleted, and provides a relatively wide current path. The subsidiary semiconductor regions establish a relatively high potential difference near the gate regions so that the distance between the gate regions can be made

substantially small. In case the subsidiary semiconductor regions are provided around the gate regions, the built-in potential at the junction will become large so that, even at the time of forward biasing, the minority carrier injection from the gate to the channel will become small. Also, this composite channel structure can be effectively applied to recessed gate device and split gate device as well [6].

There exists a bipolar transistor, which has structure actually comprising two bipolar transistors and which can operate in alternating-voltage circuit [4].

There exists a vertical bidirectional MOS-type semiconductor device, that facilitates controlling a DC current and an AC current at a relatively low on-voltage[5]. The bidirectional MOS-type semiconductor device includes a first n-channel IGBT and a second n-channel IGBT. The first n-channel IGBT is formed of n+ type source 102, p-type base 103, an n.sup.- type substrate 101 and p-type anode 104. The second n-channel IGBT is formed of n+ type source 105, p-type base 104, an n.sup.- type substrate 101 and p-type anode 103. The operation of the second n-channel IGBT is the inversion of the operation of the first n-channel IGBT. The first n-channel IGBT makes a current flow from a first terminal 106 to a second terminal 107. The second n-channel IGBT makes a current flow from second terminal 107 to first terminal 106.

summary of the invention

The advantage of the offered transistor is that it have a high technical characteristics: a high current density, a high switch power and a very low on-voltage. It can operates in both constant-voltage circuits and alternating-voltage circuits, for example 120 V and more (breakdown voltage is as a rule 1÷2kV), which means that it can be all three closed, open or latch at any voltage polarity. The thick channel connected to a separate electrode provides increasing latch current of the transistor and simplification of many circuits, which use the transistor.

This result is achieved by disposing elements of a bipolar static induction transistor on both sides of a lightly doped silicon monocrystal substrate having a donor concentration of about 10^{14} cm.⁻³: an epitaxial layer having a donor concentration of about 10^{17} cm.⁻³ is disposed on both sides said substrate; a p+ gate, n+ sources and n-channels are disposed on both sides said substrate; one channel of a multielement structure is thicker than the other normally-off channels on both sides said substrate.

This result is achieved by disposing elements of a bipolar static induction transistor on both sides of a lightly doped silicon monocrystal substrate having a donor concentration of about 10^{14} cm.⁻³: an epitaxial layer having a donor concentration of about 10^{17} cm.⁻³ is disposed on both sides said substrate; a p+ gate, n+ sources and n-channels are disposed on both sides said substrate; one channel of a multielement structure is thicker than the other normally-off channels on both sides said substrate; said channel is connected to a separate electrode on both sides said substrate.

This result is achieved by disposing a layer of a doped n+ type polysilicon on the silicon monocrystal surface on both sides of said substrate.

The offered transistors and transistor-triacs can be applied for generation, transmission and use of electric energy within a very broad range of power: from the control of electrical soldering to the control of most powerful turbogenerators and thermonuclear stations. They are effective for designing electronic transformers, power supply units, and controllable power transmission lines. In the latter case transistor-triacs can be connected in series, which will allow to easily create high voltage system with operating voltage 10÷6 V and more which can be controled either light signals or wireless. These transistors can be most widely used in the devices aimed at defending people from electric shock. They can also be used in a high speed information transmitter on an electric network. They can also be used in systems with the unipolar power supply transmitting energy in both directions – both from a source to a load (rasonator) and from the load to the source. It will make it possible to increase circuit efficiency with the voltage drop between a drain and source of the open transistor as a rule not exceeding 0.5 V and, if necessary, it can be highly

close to zero. The voltage drop between a drain and source of the latched transistor-triac equals about 1V.

For manufacturing offered transistors one uses a lightly doped n.sup.- type substrate of monocrystal silicon with long life time. The structure of the offered transistor is symmetric which means that on both sides of the substrate with the donor concentration of about 10^{14} cm.^{sup.-3} there are the epitaxial layer with the donor concentration of about 10^{17} cm.^{sup.-3}, areas of a p+ gate, a n+ sources, an ordinary channel and a thick channel as well as the electrodes of gate and sources (drains). Owing to the structure symmetry, the output voltage-current characteristics of the transistor are symmetric and are in the first and the third quadrants. Because of this, the source and drain of the transistor can change places and the transistor can operate in alternating voltage circuits of supply pressure of 120 V and more which simplifies many circuits and besides the transistor can be applied in the circuits which cannot be produced with any other types of transistors.

If threshold voltage of the channel near the drain equals about 0.6 volt the device can not be closed; open or latched only. If threshold voltage below than 0.5 volt the device can maintain high voltage if applied voltage have been changed slowly. Device operates as transistor-triac. If the threshold voltage equals approximately 0.2 volt device operates as transistor. The threshold voltage of thick channel have to equal about zero volt or below zero.

Let potentials of the gates are equal to potentials of the source and drain accordingly. Let applied voltage have been increased abruptly. The electrons flowing to the drain electrode can cause emission of the holes from the gate, disposed near the drain. The holes flow to the gate, disposed near the source. Part of the holes flow into the channel and causes the flow of the electrons to the drain. So, there is a positive feedback in the device. Device is latched. On-voltage of the latched device is more than on-voltage of the open transistor. The latch current depends on the channel resistance for the electron current, in the first place from a donor concentration in the channels, a channel length, a threshold voltage.

Introduced in the structure the thick channel provides all four increasing of the latch current, the operation of the sequently connected transistors, the determination of polarity and the control over a charge and discharge of the lightly doped area (fig.16,fig.17,fig.18,fig.20). A threshold voltage of the thick channel is lower than that of the ordinary channel. Thickness of thick channel (fig.5,fig.7,fig.8) have to be bigger than one (fig.6) under other conditions being equal. Algorithm of control of the offered transistor under typical circumstances is more complicated than that of the transistor described above [3]. Though the structure of the transistor is symmetric the operating duty of the channel that is near the drain of the transistor essentially differs from the operating duty of the channel that is near its source. The electrical field reduces the concentration of holes in the former and increases their concentration in the latter. Owing to this, the hole concentration along an axis perpendicular to surface is trapezoidal in zero approximation. It puts certain restrictions both on the design parameters of BBSIT and on designing of circuits in which these transistors are applied.

To prevent the feedback it is necessary to provide so that electrons might flow to the drain free. It depends both on a control circuit and on the construction of the transistor. The parts of the control circuit are represented on fig.16 and fig.17 of the application. Electrons might flow to the drain through open transistor 66 or 71 or backward Esaki diodes. The construction of the transistor provides the way for electrons to the drain through the thick channel while transistor is closed or is being switched off. The potential of the thick channel drain electrode has to be positive or zero or little negative relative to the potential of the drain electrode of ordinary channel. The high drain voltage extracts electrons from the thick channel which is disposed near the source. The potential of the thick channel source electrode has to be positive so that the thick channel is closed. It is allowed that the potential of the thick channel source electrode might equal zero. In one embodiment (fig.14) the thick channel source electrode has been connected to the ordinary channel source electrode.

When polarity of the applied voltage changes, the source and drain change places, and the

potentials of the thick channel electrodes should be changed accordingly so as the transistor is to remain closed. In this case the transistor can maintain voltages up to several kilovolt depending on parameters of the lightly doped area, in the first place from the thickness and number of donors between the gates as well as from performance of the channel and an edge termination structure. To prevent an avalanche breakdown near the edge of the substrate, to decrease on-voltage, to increase speed of response and current density one might use a rib of rigidity of definite dimensions (fig.19). The channels of the transistor have to dispose in the recess bottom. In this case the avalanche breakdown can occur on the gate boundary near the edge of the recess bottom or near the edge of the thick channel depending on the parameters.

Another voltage on the gates is about 0.8 V relatively of the source and drain which are nearby. It provides the opening of the channels and hole emission into the channels and lightly doped area. The emission of holes to the lightly doped area is followed by electrons from the transistor source which makes the hole concentration and electron concentration practically the same and may reach the magnitude of $10^{17} + 10^{18} \text{ cm}^{-3}$ and more; resistance of the transistor drops abruptly due to conductivity modulation and the voltage between the drain and source of the transistor as a rule does not exceed 0.5 V at current density $\approx 1000 \text{ A cm}^{-2}$ (the thickness of the substrate is decreased by etching). There is a smoothly lowering voltage on the gate which is near the source of the transistor during the switching of the transistor from on-condition to off-condition, owing to extraction. To decrease the loss of switching off the voltage on the gate which is near the drain of the transistor should be remain during the first part of time of switching off (approximately 10^{-6} sec). It is desirable a hole emission into the lightly doped area during first part of time of switching off (extraction out holes exceed emission into one).

There are different operating duties of transistor on-condition:

1. A hole concentration approximately is the same in the whole lightly doped area. The diffusion current is negligible. The gate disposed near the drain of the transistor emits holes into the channel and lightly doped area. The holes drift to the source of the transistor and are extracted by the gate disposed near the source. The electrons drift to meet holes – from the source to the drain of the transistor. The electron concentration equals approximately hole concentration. The electron current is 3 times bigger, than the hole current, owing to the electron mobility is 3 times bigger. The features of operation duty – a low current amplification factor, a high speed response.

2. A hole concentration near the source of the transistor is essentially bigger than the one near the drain (trapezoidal distribution). Owing to this, a hole current consists both a hole diffusion, directed from the source to the drain and a hole drift, directed from the drain to the source. The hole current can be for example equal to zero (zero approximation). An electron concentration approximately equals the hole concentration. An electron diffusion current and the electron drift current flow in the same direction – from the drain to the source. So almost all the current is transferred by electrons on the way of which there are almost no potential barriers and besides on the greatest part of the way the concentration of impurity is small and, correspondingly, the dispersal of carriers on impurities is small and the mobility of carriers is high as well as the concentration of holes near the drain is high. As a result, the transistor has an unusually low resistance on condition and this permits the high density current to flow at a low potential difference between the drain and the source. Gate currents depend on operation duty: first of all the recombination holes and electrons in the source, drain and gates define gate currents. Big hole currents flow through gates at the switching over of the transistor only: at an opening of the transistor by emission of holes from gates into lightly doped area and accumulation of holes; at a closing one by discharge of holes (extraction).

To increase all three operating and latch currents of the transistor and voltage which can be blocked, the offered BBSITs should have the channel with a low resistance. To this end, the thicknesses of the channels should be small and the impurity concentration near the gate should be high enough so that the electronic current flowing near the gate could not cause a large voltage drop which, in turn, could lead to emission of holes. To meet these requirements, it is desirable to grow an epitaxial layer with donor impurity concentration being about 10^{17} cm^{-3} on the

surface of the lightly doped substrate having the donor impurity concentration about 10^{14} cm.⁻³, and to have an equipment with higher resolution than is generally used for manufacturing other BSITs. The distance from the boundary of the epitaxial layer to the gate should be about 10.⁻⁵ cm. The other variant – implantation of both donor and acceptor in the gate and double drive-in diffusion ones to provide thin layer donor impurity near the gate including the channel. On the surface of a monocrystal silicon a layer of a polysilicon may be disposed that would help to form the elements of the transistor: the gate, the sources, the channels and the electrodes.

A solitary pulse current density can be several times bigger, tending to 10000 a cm.⁻² and more, if low resistance metal layers are disposed on the electrodes. The maximum pulse current is bigger than the latch current. Auger recombination restricts the carrier density and the current amplification factor. In this case the hole concentration is approximately the same in the whole lightly doped area. The influence of diffusion currents is negligible. The offered transistors can control power greater than any other types of transistors all over the world.

There are several different ways of using the thick channel. One of them is reported below. The control signals on the gates of the transistor should depend both on a polarity of the supply voltage (as a rule, it is alternating voltage with the frequency 50-60 Hz) and on the voltage applied at the moment to the transistor; two thick channels with small current have been introduced to help to determine the value and the polarity of the voltage on the transistor at that moment. Signals from these channels are transmitted to the control circuit which produces control signals to the gates. Besides, potentials and currents applied to electrodes of thick channels with control circuit are changing the operating duty of the transistor and the transistor-triac themselves. As a rule, the thick channel source electrode occupies not more than 20% of square of the ordinary channel source electrode.

It is desirable to dispose driver transistors on the chip above the main one. Most suitable transistors for the driver are low-voltage bipolar mode field effect transistors. Due to a small size, they have sufficiently low resistance on-condition, high gain and high speed response to control a power transistor. Parts of the control circuit on either side of the chip can be controlled by light signals or by wireless.

In a zero approximation, the offered transistor does multiplication of voltages applied to the transistor gates and drains and can be considered as double-band modulator and can be used, for example, to control polarity of rectified voltage.

Apart from the main purpose of application, that is using the device as a completely controllable power bidirectional key, the device can be used as transistor-triac; the control over both hole emission into and extraction out the lightly doped area are used, as well as current feedback for the control over emission (for example, latch in the construction of high voltage breaker). The current feedback provides the hole emission from the gate, which is near the drain of the device, if the resistance of the channel is high and the control circuit provides it (fig.18,fig.20).

The transistor with an offered combination of features is unknown, therefore the offered transistor corresponds to a criterion "novelty".

The offered combination of features does not obviously follow from the engineering level, technical performances does not known from prior art, therefore the transistor corresponds to a criterion "invention level".

The purpose of the invention and the means and methods of its realization are indicated in the application documents, its purpose being realizable,—which means there is "industrial applicability".

brief description of the drawings

Inventions is explained with nineteen drawings.

Fig 1 represents a semiconductor device with copper gate electrode (prior art).

Fig 2 represents a field effect transistor structure (prior art).

Fig 3 represents a bidirectional semiconductor device structure (prior art).

Fig.4 represents a power transistor-triac structure with two p-channel transistors.

Fig.5 represents a power normally-off transistor structure with two lowpower normally-on channels; implantation of both donor and acceptor in the gate and double drive-in diffusion ones provide thin layer donor impurity near the gate including the channel.

Fig.6 represents a power normally-off transistor structure with two lowpower normally-on channels; gates, sources, channels are disposed in epitaxial layers.

Fig.7 represents a power normally-off transistor structure with two lowpower normally-on channels and copper electrodes.

Fig.8 represents a power transistor-triac structure.

Fig.9 represents planar view of the offered transistor (without sequential connection) or the offered transistor-triac suitable for sequential connection. (Scale has not been kept. One of several variants; for illustration only).

Fig.10 represents a deposition of contact pads (one from several variants; for illustration only).

Fig.11 represents a construction of transistor leads (one from several variants; for illustration only).

Fig.12 represents planar view of the offered transistor or transistor-triac (fig.4) suitable for sequential connection. (Scale has not been kept. One of several variants; for illustration only).

Fig.14 represents a symbolic image offered of the power normally-off transistor with two thick channels (threshold voltage of thick channel have to equal about zero volt).

Fig.15 represents a symbolic image offered of the power normally-off transistor with two thick channels.

Fig.16 represents offered transistor with a part of the control circuit (one from several variants; for illustration only).

Fig.17 represents the offered transistor with a part of the high voltage control circuit (one of several variants; for illustration only).

Fig.18 represents a part of the circuit of the high voltage breaker with offered transistor-triacs (one of several variants; for illustration only).

Fig.19 represents the substrate structure with the ribs of rigidity (one of several variants; for illustration only).

Fig.20 represents a part of the circuit of the breaker with offered transistor-triacs (one of several variants; for illustration only).

detail description of the preferred embodiment

Semiconductor device fig.1 comprises substrate 1, gate oxide film 2, gate electrode (polysilicon) 3, trench 4, barrier film 5, copper gate contact 6, isolation 7, source 8, drain 9, silicide contacts of source and drain 10.

Bipolar static induction transistor fig.2 comprises substrate 11, drain electrode 12, epitaxial layer 13, gate 14, gate electrode 15, source 16, channel 17, source electrode (n+-type polysilicon) 18, source contact 19, isolation 20.

Bidirectional semiconductor device fig.3 comprises substrate 21, n+ type source 22, p-type base (anode) 23, p-type anode (base) 24, n+ type source 25, terminals 26,27.

Bidirectional bipolar static induction transistor-triac (IC) fig.4 comprises lightly doped n.sup.- type substrate (area) 28, p+ type gates 29, silicide gate electrodes 30, thick n-channels 32, ordinary n-channels 36, sources 37, source electrodes (n+ type polysilicon) 38, silicide source contacts 39, isolation 40, n-type layers 41, p-channel transistor gates 106, p-channels 107, source electrodes (p+ type polysilicon) 108, silicide source contacts 109.

Bidirectional bipolar static induction transistor fig.5 comprises lightly doped n.sup.- type substrate (area) 28, gates 29, silicide gate electrodes 30, thick channels 32, thick channel sources 33, thick channel source electrodes (n+ type polysilicon) 34, silicide thick channel source contacts 35, ordinary channels 36, ordinary channel sources 37, ordinary channel source electrodes (n+ type

polysilicon) 38, silicide ordinary channel source contacts 39, isolation 40, n-type layers 41.

Transistor has created by the implantation of both the donor and acceptor in the gate and double drive-in diffusion to provide the thin layer donor impurity (about $10 \cdot 10^{12} \text{ cm}^{-2}$) near the gate including the channel.

Bidirectional bipolar static induction transistor fig.6 comprises lightly doped n.sup.- type substrate (area) 28, gates 29, silicide gate electrodes 30, thick channels 32, thick channel sources 33, thick channel source electrodes (n+ type polysilicon) 34, silicide thick channel source contacts 35, ordinary channels 36, ordinary channel sources 37, ordinary channel source electrodes (n+ type polysilicon) 38, silicide ordinary channel source contacts 39, isolation 40, epitaxial layers 42.

Thickness of the transistor channel equals about 1.7.times. thickness of the depletion layer at built in potential, thickness of the thick channel equals about 1.9(fig.14) or 2.2.times. of the one (fig.15).

Bidirectional bipolar static induction transistor fig.7 comprises lightly doped n.sup.- -type substrate (area) 28, gates 29, copper (Cu+barrier film TiN) gate electrodes 30, thick channels 32, thick channel sources 33, thick channel source electrodes (n+ type polysilicon) 34, copper thick channel source contacts 35, ordinary channels 36, ordinary channel sources 37, ordinary channel source electrodes (n+ type polysilicon) 38, copper ordinary channel source contacts 39, isolation 40, n-type layers 41.

Bidirectional bipolar static induction transistor-triac fig.8 comprises lightly doped n.sup.- type substrate (area) 28, gates 29, silicide gate electrodes 30, thick channels with nonuniform distribution of donors 32, thick channel sources 33, thick channel source electrodes (n+ type polysilicon) 34, silicide thick channel source contacts 35, ordinary channels with nonuniform distribution of donors 36, ordinary channel sources 37, ordinary channel source electrodes (n+ type polysilicon) 38, silicide ordinary channel source contacts 39, isolation 40, n-type layers 41.

Transistor-triac have a low holding current. It has created by the implantation of both the donor and acceptor in the gate and double drive-in diffusion to provide the thin layer donor impurity (about $5 \cdot 10^{11} \text{ cm}^{-2}$) near the gate including part of the channel.

Planar view of the offered transistor fig.9 comprises source contact of ordinary channel 43, gate electrode 45, source contact of thick channel 46.

This construction permits to create transistor-triacs which can be connected seriesly as well as transistors (There is danger of destroying seriesly connected transistors manufactured accordingly fig.9 during transistors is being switched off unlike transistors manufactured accordingly fig.12).

Planar view of the offered device fig.10 comprises contact pad of ordinary channel 47, contact pad of gate 48, contact pad of thick channel 49.

A construction of the transistor leads fig.11 comprises chip with contact pads 50, source leads of ordinary channels 51, gate leads 52, source leads of thick channels 53, isolation 54.

Planar view of the offered transistor fig.12 comprises source contact of ordinary channel 43, gate electrode 45, source contact of thick channel 46.

Dimentionions of the different parts of the thick channel have been chosen taking into consideration an operation of the automatic control system of the keys to remove possibility of an autogeneration. The seriesly connected transistors manufactured accordingly fig.12 can be switched off without destroying unlike transistors manufactured accordingly fig.9.

Symbolic image of power normally-off transistor with two lowpower thick channels fig.14 comprises gates 55,56; sources of a power transistor 58,59 (threshold voltage of thick channel have to equal about zero volt).

Symbolic image of power normally-off transistor with two lowpower thick channels fig.15 comprises gates 55,56; sources of lowpower channels 57,60; sources of a power transistor 58,59.

Fig.16 comprises offered transistor 61, hole emission key 62, hole discharge (extraction) key 63, electron discharge key 66, amplifier with nonlinear feedback (polarity fixture) 64,65,66; hole emission key 67, hole discharge (extraction) key 68, electron discharge key 71, amplifier with nonlinear feedback (polarity fixture) 69,70,71; (transistors 62,63,66,67,68,71 – low-voltage

bipolar mode field effect transistors).

Fig.17 comprises the offered transistor 61, hole emission key 62, hole discharge (extraction) key 63, electron discharge key 66, amplifier with nonlinear feedback (polarity fixture) 64,65,66; diodes 72,73, hole emission key 67, hole discharge (extraction) key 68, electron discharge key 71, amplifier with nonlinear feedback (polarity fixture) 69,70,71; diodes 74,75; (transistors 62,63,66,67,68,71 – low-voltage bipolar mode field effect transistors).

If the drain voltage exceeds a threshold voltage it extracts electrons from the thick channel through the group of diodes 72,73 or 74,75 and prevents further increasing of the voltage on the device. Seriesly connected transistor-triacs allow to easily create high voltage system with operating voltage 10.sup.6 V and more with a control with light signals or by wireless.

Fig.18 comprises button "start" 76, button "break" 77, reformer 78, transformer 79, offered transistor-triacs 82,87; p-channel low-voltage bipolar mode field effect transistors 81,83,86,88; Schottky diodes 80,84,85,89; backward Esaki diodes 90,93,94,97; resistors 91,92,95,96,105; switch 98, solenoid 99, mobile contact 100, immobile contacts 101÷104.

Let the switch 98 be off. After the button "start" 76 is pushed, the reformer 78 switches on the solenoid 99 synchronously with alternating voltage. The mobile contact 100 is closed to contact 104 in several milliseconds and a small current flows to the contact 103 and the transistor-triacs 82,87 through resistor 105. In several milliseconds the mobile contact 100 is closed to the contact 103 and the transistor-triacs 87,82. The reformer 78 sends the pulse on the transformer 79 in one cycle of voltage the moment the voltage zero crossing is detected. The transistor-triacs 87,82 are switched on and the current begins to flow through the contacts 101,100,103. P-channel transistors near the drains of power transistor-triacs are open, but p-channel transistors near the sources of power transistor-triacs are closed. In several milliseconds the contacts 100,102 are closed and the current flows to the load by the shortest way. Thus, the switching on takes place without arcing.

Let the alternating current flow to the load through the contacts 101,100 and 102. After the button "break" 77 is pushed the solenoid 99 disconnects the contacts 100,102 without synchronizing with voltage. The current flows between the contacts 101,100,103 and the transistor-triacs 87,82 for several milliseconds. After the current is decreased to holding current the operating duty of the devices are changed to unlatched. P-channel transistors 81,83,86,88 help to discharge power transistor-triacs 87,82. After the current zero crossing takes place the devices 82,87 are switched off and the current is switched off. In several milliseconds the solenoid 99 disconnects the contacts 100,103,104. Thus, the switching off takes place without arcing within one cycle of voltage.

Fig.19 comprises the operation part of the substrate 106, ribs of rigidity 107, recess 108.

The ribs of rigidity increase a mechanical durability of the substrate and permit to decrease the thickness of the operation part and to improve the main performances of the transistor.

Fig.20 comprises button "start" 76, button "break" 77, reformer 78, transformer 79, offered transistor-triacs 82,87; p-channel low-voltage bipolar mode field effect transistors 81,83; Schottky diodes 80,84; backward Esaki diodes 90,93; resistors 91,92,105; switch 98, solenoid 99, mobile contact 100, immobile contacts 101÷104.

The p-channel low-voltage bipolar mode field effect transistors 81,83 can be manufactured as lateral and disposed over(under) the thick channels of power transistor-triac.

Improvement of characteristics of the transistor can be achieved by cooling of one.

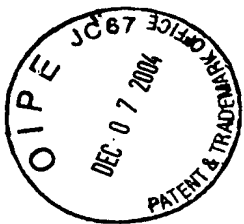
While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that the foregoing and other changes in form and detail may be made therein without departing from the spirit and the scope of the invention.

AUTHOR:



12.05.2004

EDLIN S.D.



References

1.Jung Jong-Wan. Method for fabricating semiconductor device with copper gate electrode. U.S.Patent No.6479357. H01L 021/336. Priority Feb 29, 2000.

2.Edlin S.D. JFET transistor and method for manufacturing the same. R.F.Patent No.2102818. H01L 29/80. Priority Apr.15.1992.

3.Edlin S.D. The application for issue of the patent of RF No.2000100080. A bipolar static induction transistor. H01L 29/06. Application mailed 01.05.2000.

4.Smoliansky B.A. et al. Author's certificate USSR No.736807. H01L 29/70. Priority 01.22.1979.

5.Aizawa Yoshiaki et al. Semiconductor device. JP Patent No.3352840. H01L 29/78. H03K 17/56. H03K 17/68. Priority 14.03.1994.

6.Nishizawa Jun-ichi. Static induction type semiconductor device with multiple doped layers for potential modification. U.S.Patent No.4364072. H01L 029/80. Priority Mar 17, 1978.